Components Systems Software Services

TeleSoft NEWS

WINTER 2003

IN THIS ISSUE

A WORD FROM THE FIRM

In the second half of 2003, we were delighted to announce the IPOs of **SigmaTel** (Q3) and **Provide Commerce** (Q4), and to invest in **LogLogic** with Sequoia Capital. LogLogic specializes in real-time log information processing. LogLogic's goal is to establish itself as a leader in real-time log processing for firewalls and other critical elements. It has paying customers in North America and Europe, including Fortune 500 companies.

Congratulations to our existing portfolio companies on new financings: **CreekPath** raised $16+ million from AG Edwards, NEA, Sequel, and TeleSoft; **Calient** raised $20 million from Enterprise, Sofinnova, SDL, and TeleSoft; and **Aarohi** raised $13+ million from Infineon, Kennet, McData, and TeleSoft.

As the new year progresses, the two- to three-year downward slide in technology spending appears to have hit bottom with most analysts projecting improvements in 2004, barring negative macroeconomic or global surprises. IPO activity picked up over the last several quarters. M&A activity also increased as some tech sectors consolidated and large vendors filled in product gaps (gaps which were created from cutbacks over the last two years). Looking forward, several technology themes, which emerged last year, are expected to continue to gain momentum: the convergence of consumer digital media, increasing activity in next-gen access, overall storage management, broader wireless LAN deployment, continued emphasis on security, and the continued shift to modular, open source platforms.

Thanks also to all the speakers and attendees at TeleSoft's Ecosystem Meeting in October. Please save the date for this year's meeting on October 28–30, 2004!

— Arjun Gupta

Lynx Photonic Networks' LightLEADER™ 3000 series.
For more information on the latest products and services of our portfolio companies, see Portfolio News on page 7.

Save the Date

OCTOBER 28–30, 2004

TeleSoft Partners' Annual VC Ecosystem Meeting

Half Moon Bay, California

A special thanks to all the keynote speakers at TeleSoft's 2003 Ecosystem Meeting:

Robert Buxton, CIBC
Sureel Choksi, Level 3
Mark Christensen, Intel
Mike Danaher, WSGR
Paul Deninger, Broadview
Dean Douglas, IBM
Doug Garland, Yahoo!
Kris Hagerman, Veritas
Ammar Hanafi, Cisco
Stephen Minton, IDC
George Polk, The Cloud
William Raduchel, AOL
Michael Rouleau, TW Telecom
Roland Wolfram, Nike

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From the Front Lines

Straining Moore's Law

For decades, manufacturers have steadily shrunk the size of transistors in accordance with Moore's Law, which dictates that the number of transistors on a chip doubles every eighteen to twenty-four months. The decreasing size, or scaling, has led to dramatic increases in semiconductor performance. The 90nm process in production today is the next generation after the 130nm process, which Intel is using now to make the bulk of its microprocessors (see figure 1). By 2007, Intel plans to build a one billion transistor chip using a 45nm generation process. Despite the great success of Moore's Law, scaling is increasingly questioned as the best method for improving semiconductor technology. One issue is scaling increases chip power consumption, which is an important consideration for a variety of modern electronics applications. In addition, scaling has reached the point of diminishing returns with high dollar investments for minimal technical advance. The industry is now looking to achieve as much or more progress by changes in the fundamentals of chip materials.

Mayank T. Bulsara, co-founder and chief technology officer of AmberWave Systems Corporation, contributed this issue of "From the Front Lines." It focuses on the metrics to consider for the commercialization of strained silicon technology. The technology takes advantage of the natural tendency for atoms inside compounds to align with one another. When silicon is deposited on top of a substrate with atoms spaced farther apart, the atoms in silicon stretch to line up with the atoms beneath, stretching—or "straining"—the silicon. In the strained silicon, electrons experience less resistance and flow faster, increasing semiconductor performance and decreasing power consumption in semiconductors. The increased performance adds more horsepower to enterprise and Web applications. However, near-term emphasis may be on lower power dissipation than increased processor speeds. Future power-efficient chips could translate to advanced handheld features such as higher quality video and voice-driven interfaces.

In the strained silicon, electrons experience less resistance and flow faster, increasing semiconductor performance and decreasing power consumption in semiconductors.

Strained Silicon: Key Metrics for Commercial Implementation

The silicon wafer, the ubiquitous platform for the microelectronics industry, has for many years undergone tremendous improvements, among them increased wafer size and greater levels of crystalline quality. Even though wafer manufacturers have continued to provide highly engineered products to the silicon industry, advances in transistor integration have traditionally dictated the system level performance and highest-end product gains. This has led to a cost structure for silicon product manufacturing that favors asset allocation for lithography and other transistor integration advances, while investments in silicon substrate engineering are secondary.

Recently, advances in alternative silicon substrate technologies that provide extensive benefits for silicon-based products have made the choice of substrate technology a much more strategic decision. Thus,

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FIGURE 1: ADVANCING MOORE'S LAW

	1999	2001	2003	2005	2007
Transistors	28M	42M	>55M	Introduction of **STRAINED SILICON** technology	
Processor Speed	0.5-0.73 GHz	1.4-1.5 GHz	2-3 GHz		
Process Technology	0.180µ	0.130µ	0.090µ	0.065µ	0.045µ

From the Front Lines

Straining Moore's Law

manufacturers must revisit their planning for product deployment and the extent of their investment in substrate technologies.

Strained silicon technology holds much promise for enhancing silicon products, and many manufacturers are evaluating its potential for improving their products. However, since the insertion of advanced substrate technologies in mainstream silicon products is in the early stages (i.e., volume-cost curves for substrates and end-product enhancements are not widely understood), it is difficult for fabless semiconductor companies and chip manufacturers to determine the cost-benefit analysis of a technology like strained silicon.

In this article, substrate cost and circuit design implications are outlined as two of the key metrics that must be considered for the implementation of strained silicon products. The basic process and performance enhancement capabilities of strained silicon technology are highlighted and simple models are considered in order to understand the potential impact of strained silicon technology on the cost structure of silicon products.

It is difficult for fabless semiconductor companies and chip manufacturers to determine the cost-benefit analysis of a technology like strained silicon.

Strained Silicon Substrate Manufacturing Process and Cost

Two of the key considerations for strained silicon technology are the availability (i.e., the speed at which production volumes can be put into place) and the cost of strained silicon substrates in high volume production.

The fabrication of state-of-the-art strained silicon substrates requires a three-step process:

1. *Epitaxial deposition of a relaxed SiGe film, which is the strain-inducing template for a subsequent strained silicon film.* Properly executed, the deposition of the relaxed SiGe film ensures a film of very high crystalline quality, but also results in a rough surface morphology.
2. *Reduction of the surface roughness resulting from the deposition of the relaxed SiGe film.* This is typically accomplished by techniques such as chemical mechanical polishing (CMP), which planarize and polish the surface.
3. *Epitaxial deposition of the strained silicon device layer.* This provides the performance-enhancing film that serves as the device channel layer.

This total thickness of the strained silicon thin film structure is on the order of 2-4 mm. By comparison, the traditional epitaxial silicon film on silicon substrates found

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TABLE 1: MANUFACTURING PROCESS FLOWS FOR SILICON SUBSTRATE TECHNOLOGIES

Step	Epitaxial Silicon Process Flow	Strained Silicon Process Flow	Bonded SOI Process Flow
1	Prepare bulk silicon wafer (smooth wafer surface)	Prepare bulk silicon wafer (smooth wafer surface)	Prepare bulk silicon wafer (smooth wafer surface)
2	Provide epitaxial layers	Provide epitaxial layers	Provide buried oxide
3		Smooth wafer surface	Perform H^+ implant
4		Provide epitaxial layers	Bond to 2nd handle wafer
5			Perform split and strengthening anneals
6			Smooth wafer surface

From the Front Lines

Straining Moore's Law

in most advanced logic processes is also typically 2 mm thick.

In terms of process complexity, table 1 benchmarks the strained silicon process flow against a traditional epitaxial silicon process flow and a bonded silicon on insulator (SOI) process flow. First, note that the base equipment/processes required for traditional epitaxial silicon film processing can be readily applied to strained silicon substrate production. Thus, rapid ramp-up of production of strained silicon substrate supply is straightforward since no additional infrastructure is required. Second, it is well known that 200 mm epitaxial silicon and 200 mm bonded SOI wafers have attained price-volume curves that make their application economical (typically 200 mm epitaxial silicon wafers cost $65/wafer while 200 mm bonded SOI wafers typically cost $300-$400/wafer). The volume production of strained silicon wafers clearly falls within the same economic constraints of epitaxial silicon and bonded SOI wafer manufacturing. Currently, strained silicon wafers cost more than their counterpart substrate technologies because the volume and production process maturity have not attained the comparable levels. Thus, the equipment depreciation cost per wafer dictates a higher development level cost for strained silicon wafers at present. With modest assumptions for equipment utilization (i.e., reuse of invested capital and high throughput processing) and volume consumption, a strained silicon substrate cost of less than $200 per 200 mm wafer is a reasonable projection.

TABLE 2: COST ESTIMATES FOR NEW PRODUCTION TECHNOLOGY LAUNCH

Node	Mask Set Cost	Strained Silicon Substrate Cost (200 mm substrates)	Process Cost/ Wafer
130 nm	$0.6M	$200	$2000
90 nm	$1.5M	$200	$2200
65 nm	$2.0M	$200	$2400
45 nm	$3.0M	$200	$2600

Tradeoffs for Chip Manufacturing

With system level benefits arising from many segments of the supply chain—from the substrate level to back-end metal interconnect technology—there are more choices involved in a chip product launch. The ability of a manufacturer to pick the optimum answer in terms of performance-cost structure will dictate its competitiveness in the modern semiconductor industry.

Table 2 provides the basis for a simple model for examination of product manufacturing costs.[1] The estimates are conservative and merely allow a comparison of technology options. However, two key assumptions are made for the model that render it an approximate best-case scenario for production costs:

1. Product yield costs (i.e., yield learning costs and final attainable yield) are considered to be equivalent from node to node, which is unlikely given the process complexities that are introduced at some of the most advanced nodes.
2. Products do not experience any redesign, and mask costs are not multiplicative, an optimistic scenario for the most highly integrated products.

To elucidate the need to further tailor technology choices for each product application, the basis of manufacturing costs in table 2 can be applied to some examples of product launch.[1] Referring to table 3, the effect of amortizing the cost of mask sets for a given product volume plays an essential role in determining the best technology choices for a product family launch. Clearly, at moderate volumes (10,000's) of wafers

[1] Model adapted from presentation by Dr. Helmut Tews of Infineon Technologies at Semicon Europa 2003.

CONTINUED ON PAGE 5

the cost of mask sets is very high, while for the extremely high volume applications the impact of lithography is much less (again, assuming that yields and need for redesign are not more problematic). In either case, a production level strained silicon substrate cost would be reasonable given the benefits and costs of comparative approaches (e.g., it accounts for 9 percent of the total cost for the worst case of a 100,000 wafer start product running at the 130 nm node, and for moderate volumes levels and more aggressive technologies, 5–6 percent of the total wafer cost would be typical).

Circuit Design with Strained Silicon

Strained silicon transistors have been demonstrated to provide approximately 25–30 percent improvement in NMOS drive current in tandem with 5–10 percent improvement in PMOS drive current, which can be used to either increase the speed or decrease the power consumption of integrated products. In conventional silicon technology, it is well known that NMOS transistors have a slightly greater than 2X performance advantage over their PMOS counterparts. This leads to design considerations that require optimization of the transistor layout to account for the imbalance in NMOS and PMOS drive currents. Strained silicon transistors widen the gap between NMOS and PMOS by about 20 percent; however, the raw performance of each is separately enhanced.

Substrate cost and circuit design implications are two of the key metrics that must be considered for the implementation of strained silicon products.

A common question that arises regarding strained silicon technology is the effect of strained silicon substrate insertion into production with preexisting designs that have not accounted for the extra imbalance between NMOS and PMOS transistors (i.e., are redesign costs required to see the benefits of strained silicon technology?). Figure 2 shows that even without any modification to a preexisting design, strained silicon CMOS circuits provide advantages in power consumption (34 percent reduction) and propagation delay (17 percent increase in speed). Note that the transistor optimization for this publication was not complete, hence even greater advantages will be demonstrated with further development.

Without any modification to the ring oscillator layout, strained silicon technology benefits are compelling, but it is likely that with modification to the circuit layout even more performance benefits can be achieved. Since minor product redesigns occur frequently at process node transitions for other technological demands, the maximum performance benefit of strained sili-

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TABLE 3: COST BREAKDOWN ESTIMATES FOR DIFFERENT SCALE PRODUCT LAUNCHES

Node	Process Cost/Wafer	Mask Cost/Wafer 1,000 Wafer Starts	Mask Cost/Wafer 10,000 Wafer Starts	Mask Cost/Wafer 100,000 Wafer Starts	Strained Silicon Substrate Cost
130 nm	$2000	$600	$60	$6	$200
90 nm	$2200	$1,500	$150	$15	$200
65 nm	$2400	$2,000	$200	$20	$200
45 nm	$2600	$3,000	$300	$30	$200

con will be easily utilized. In practice, circuit and library designers will choose the best path for their application with the foreknowledge that strained silicon technology is flexible enough to address their product needs at various levels.

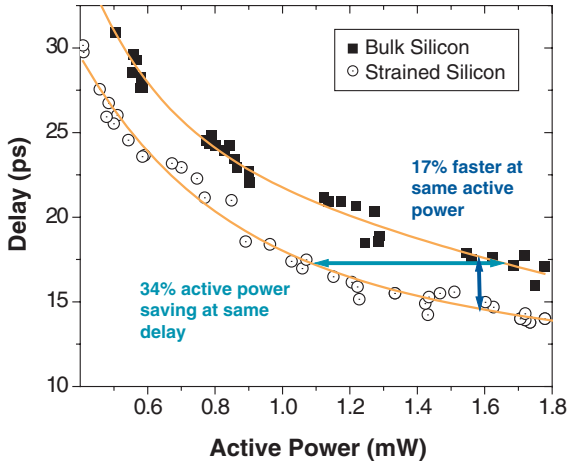
Summary: Improved Performance Using Existing Process Methodology

Advanced silicon substrate technologies are establishing attractive positions for mainstay CMOS product application, but the industry is currently grappling with the methods to evaluate the economic and performance tradeoffs.

Strained silicon technology is at the crossroad where manufacturers can establish confident projections for its cost and its performance. A key criterion for cost is the ability to assess if strained silicon substrate technology can sustain the same economic fundamentals that traditional silicon substrate manufacturing enjoys. With no change in the process methodology and manufacturing infrastructure, strained silicon is well on its way to achieving this objective. In addition, substrate technology benefits are now just as compelling as other process-related improvements, so manufacturers have more choices for their product needs than in the past. The performance questions that arise regarding strained silicon transistor technology center on the ability to reuse existing designs to attain significant product benefits. Demonstrations have shown that a redesign need not be necessary to realize significant performance benefits with strained silicon technology.

Overall, product differentiation needs and cost-performance tradeoffs will determine the technology choices for manufacturers in the silicon industry. Strained silicon technology offers enough elasticity to manufacturers for rapid deployment at any time, and provides a range of performance benefits at attractive price points.

FIGURE 2: POWER CONSUMPTION AND PROPAGATION DELAY OF 151 STAGE, STRAINED SILICON AND BULK SILICON RING OSCILLATORS MADE WITH A PREEXISTING TEST MASK SET[2]



[2] The circuits were fabricated by UMC in collaboration with AmberWave Systems, and the results were presented at the 2003 VLSI Symposium in Kyoto.

Dr. Mayank Bulsara co-founded AmberWave in June 1998 with Dr. Eugene Fitzgerald. As chief technology officer, he works with AmberWave's engineering, marketing, and business development teams to launch directions and plans for AmberWave's technology road map. Bulsara drives and supports several aspects of AmberWave's intellectual property strategy and development initiatives. In addition, he coordinates with AmberWave's sales and marketing teams to establish and support strategic sales accounts. Bulsara originally studied under Fitzgerald, completing groundbreaking research involving the characterization and integration of lattice-mismatched III-V compound materials on GaAs and Si substrates. Bulsara has co-authored numerous patents and technical papers on the design and properties of substrates and devices. He holds a bachelor's degree in ceramic engineering from Rutgers University, and a Ph.D. and S.M. from MIT's Department of Materials Science and Engineering.

Portfolio News

Aarohi Communications

www.aarohi-inc.com

- Aarohi completes $13.5 million series B1 financing. The round was led by new corporate investors McData Corporation and Infineon Technologies and included participation from previous investors. The round brings Aarohi's total funding to date to more than $36 million (12/15/03).

FabricStream

- Aarohi introduces FabricStream to boost performance and to deliver time-to-market advantage for intelligent storage networking platforms. Fibre Channel switch maker McData will use Aarohi's ASIC in a switch slated to ship this year. Five providers of storage-management software—Alacritus, FalconStor, Incipient, Kashya, and StoreAge Networking Technologies—also will port their applications to the Aarohi FabricStream ASIC (10/21/03).

AmberWave

www.AmberWave.com

- AmberWave licenses planarization technology to Sumco for bulk strained silicon wafer manufacturing. "This makes it much easier for chip makers outside the top tier to start working with strained silicon technology to enhance their designs at 90 and 65nm," says industry analyst Dan Hutcheson (12/8/03).
- AmberWave launches third round of venture capital financing to raise $25 million to $50 million. AmberWave's investors include Hillman Company, Adams Capital Management, ARCH Venture Partners, TeleSoft Partners, and Dow Chemical. The firm has raised $45.7 million in venture capital (12/1/03).
- AmberWave enters an exclusive licensing agreement with Agere Systems for strained silicon technology (11/10/03).

BayPackets

www.BayPackets.com

- Global Crossing chooses BayPackets' Agility Network Services Platform (NSP) to enable the migration of its Account Code products and services from an existing circuit-switched network to a next-generation VoIP network. As part of this migration, Global Crossing expects to deploy BayPackets' Agility Authorization Codes application in early 2004. This will enable Global Crossing's enterprise customers to control service access and/or third-party billing (1/12/04).
- BayPackets names Dr. K.C. John as general manager and chief operating officer of BayPackets India (11/7/03).
- BayPackets launches its Agility Alliance Program, which enables application providers to easily integrate with BayPackets' NSP to deliver comprehensive solutions to service providers and cable operators. The first Agility Alliance Partners are CosmoCom, Spectel, and Sylantro Systems (11/3/03).
- BayPackets and Spectal team up to deliver conferencing applications that support circuit switched and next-generation IP networks. As part of this strategic partnership, Spectel is integrating its comprehensive set of voice and data conferencing applications that support multiservice network infrastructures with BayPackets' NSP (11/3/03).

Portfolio News

Calient Networks
www.calient.net

- Calient completes its fourth funding round, raising $20 million. New investor Sofinnova Ventures co-led the round with existing investors Enterprise Partners and TeleSoft Partners. Existing investors Storm Ventures and Van Wagoner Funds also participated, joined by new investor SDL Ventures. Due to continued interest, the company has scheduled a second closing in March 2004 to accommodate other interested investors, for up to $10 million (1/12/04).

Calix
www.calix.com/

- Calix products accounted for 70 percent of voice ports and 63 percent of DSL ports shipped on BLC platforms within North America during the third quarter of 2003, according to Infonetics Research. Broadband loop carriers (BLCs) are defined by Infonetics as packet-based devices deployable in central office and remote terminal locations capable of supporting broadband interfaces on 100 percent of rated line capacity (1/21/04).
- Calix ships Platform Release 2.1 to its 100th customer. More than 200,000 ports are installed in over 1,500 Calix C7 platforms supporting voice, data, and video service delivery to business and residential subscribers (12/8/03).

CreekPath's Suite: TechTarget Product of the Year

- Calix demonstrates live "End-to-End, IP-based Switched Video Services Delivery Over DSL" at TelcoTV. This multi-vendor demonstration included video delivery components from Amino, i3 micro technologies, Minerva Networks, Myrio, Thomson, Tut Systems, and Westell Technologies. Calix kicked off its nationwide Simplified Services Tour on enabling the video revolution in October at USTA Telecom 2003 (11/13/03).

CoSine Communications
www.cosinecom.com

- CoSine reports revenue of $4 million for the quarter ending September 30, 2003, and a net loss of $8.2 million or $0.84 per share as compared to revenue of $5.2 million and a net loss of $9.0 million or $0.93 per share in the quarter which ended September 30, 2002. The company ended the quarter with $66.9 million in cash and short-term investments (10/21/03).
- KT Corporation introduces a new DSL network aggregation application using the CoSine IPSX 9500. CoSine's new DSL capability helps KT serve its growing broadband customer base while reducing the cost per subscriber (10/21/03).
- CoSine adds Jerry Jalaba to its management team as senior vice president of worldwide sales (10/21/03).

CreekPath Systems
www.creekpath.com

- TechTarget's Storage and SearchStorage.com select the CreekPath Suite for the 2003 silver "Products of the Year" award in the Storage Management Software category (1/13/04).

Portfolio News

- Barclays, one of the largest financial services groups in the United Kingdom, chooses CreekPath's Storage Operations Management (12/3/03).
- CreekPath appoints David Lacey as chief financial officer (11/19/03).
- Cap Gemini Ernst & Young and CreekPath forge multi-year partnership. Cap Gemini Ernst & Young will resell the CreekPath Suite as well as provide consulting, integration, and implementation assistance to customers (10/28/03).
- CreekPath launches its Global Solutions Partner Program, a collection of sales and implementation tools that support marketing, sales, finance, and technical efforts. The program is tailored to meet the needs of storage service providers, storage integrators, and value added resellers (VARs). Charter members of the CreekPath Global Solutions Partner Program include North America partners Cap Gemini Ernst & Young, d-tech Corporation, Greenwich Technology Partners, and Sanz. European partners include CNT, Active Infrastructure, StorConcepts, and Intellistorage (10/28/03).
- CreekPath demonstrates its Suite 3.0 interoperability in SMI-Lab3 at Storage Networking World. The SMI-Lab3 gave customers a hands-on demonstration of the benefits that the SMI-S standard delivers for managing heterogeneous storage environments (10/27/03).

Internet Photonic's LightStack™ GSLAM (Gigabit Services Line Access Multiplexer) is a purpose-built multiservice platform that integrates transport aggregation, cross-connect functions, and optical networking to address today's access network build-outs

- CreekPath expands its European operations by adding London and Paris to its already established Edinburgh location (10/15/03).

Ikanos Communications

www.ikanos.com

- Ikanos adds Daniel K. Atler, Derek Obata, and Lionel Bonnot—all executives in the areas of finance and sales—to accelerate VDSL deployments in Asia, Europe, and Canada. Ikanos also welcomes the addition of two new board members: Roger Evans, of Greylock Ventures, and Michael Gulett, who held positions as CEO for ARC International and Paradigm Technologies as well as served as president and COO for Virata Corporation (11/11/03).
- Shipments of Ikanos's SmartLeap™ programmable VDSL-DMT chipsets have exceeded 1 million ports since volume production began less than a year ago. There has been a 200 percent increase in sales since DMT was selected as the only standard for VDSL by the standards bodies—T1E1.4 and IEEE 802.3ah EFM working groups (10/20/03).

Internet Photonics

www.internetphotonics.com

- Internet Photonics unveils a new 40 wavelength modular LightHandler optical add-drop multiplexer (OADM) designed for metro-regional optical transport networks. The LightHandler platform, which has already been deployed by one major cable operator, provides video on demand (VOD) scalability as well as other service requirements in major metropolitan cable headends (1/12/04).

Portfolio News

- Internet Photonics announces significant enhancements to its LightStack MX optical multiplexing and transport platform aimed at operators who are deploying on-demand services and converged multiservice networks (1/12/04).
- Internet Photonics is listed in CED Magazine's Broadband 50, a list of companies, technologies, people, and "categories" that have shaped, defined, and influenced the broadband industry in 2003 or are well positioned to do so in 2004 (12/1/03).
- TDS Metrocom rolls out a new private-line ethernet service with Internet Photonics' Intelligent Wavelength Platforms (11/17/03).
- Adelphia selects Internet Photonics' LightStack equipment for transport of VOD, high-speed data, and other advanced services (11/6/03).
- Buckeye CableSystem deploys Internet Photonics' equipment in a new multiservice network for VOD and commercial services (10/6/03).

Jungo

www.jungo.com

Jungo's OpenRG is intricate to the Linksys broadband router

- Jungo and SurfControl, a Web and e-mail filtering company, introduce a Web filtering software solution for residential and SOHO gateways. The new solution integrates SurfControl's Web filtering technology with Jungo's OpenRG™ residential gateway software to create a new services platform for broadband CPE (11/25/03).

Jungo's OpenRG powers this Toshiba cable modem router

- Jungo releases OpenRG v3.0, which offers new technology modules for broadband CPE manufacturers. These include OpenRG's file server for storage devices, WiFi Protected Access (WPA) for 802.11a/b/g wireless access points, Layer Two Tunneling Protocol Virtual Private Networking (L2TP VPN), and VLAN 802.1Q and 802.1P bridging (11/5/03).
- Avnet Electronics Marketing and Jungo successfully complete PCI-X compliance tests using the new PCI-X 64/133 design kit. Powered by the Xilinx Virtex-II FPGAs and the LogiCORE™ PCI-X IP Core, the new design kit will now let system designers create fully compliant, real world PCI-X applications quickly and easily (10/22/03).

Lynx Photonic Networks

www.lynxpn.com

- Lynx introduces six new models in the LightLEADER™ 3000 Product Line. LightLEADER is a small optical communications system built around Lynx's patented intelligent optical switch fabrics. The new models are an array of eight (2x2) photonic switches, two arrays of eight (1x2/2x1) photonic switches—one that allows traffic to pass through to pre-designated alternative paths during power off and one that blocks traffic during power off, an array of four (1x2/2x1) photonic switches with bi-directional switching, and a 1x4 photonic switch, which can also be used as a 4x1 (12/31/03).
- Lynx PLC-based Photonic Switch passes one of the most stringent tests in the optical communications industry to validate its endurance after repeated switching operations (12/2/03).

Portfolio News

- Digital Technology, Inc. and MCC Sales sign on as Lynx's first channel partners for the new Lynx LightLEADER family of plug-and-play photonic switches. A range of applications makes LightLEADER ideal for a broad-based network of distributors, resellers, and manufacturer's representatives and was instrumental in DTI and MCC Sales embracing the product line (11/5/03).

Matrix Semiconductor
www.matrixsemi.com/

- Dan Steere, Matrix's vice president of marketing, delivers a presentation discussing the progress and promise of 3-D at the Nikkei Semiconductor Memory Symposium in Tokyo, Japan (12/18/03).
- Matrix appoints William J. Ruehle to its board of directors. Ruehle is vice president and chief financial officer for Broadcom Corporation (10/20/03).

NP Photonics
www.npphotonic.com

- NP Photonics names Philippe Brak, formerly of Gigabit Optics, as vice president of sales and marketing (1/12/04).
- NP Photonics expands its global distribution network with the inclusion of Laser Spectronix in Korea and Laser2000 in the United Kingdom, Belgium, France, Sweden, and Germany (12/31/03).

Lynx Photonic Networks' LightLEADER™ 3000 series are small optical communications systems—built around Lynx's patented intelligent optical switch fabrics

OnFiber Communications, Inc.
www.onfiber.com

- OnFiber announces that it is supplying Shutterfly, an independent photo service, with a critical element in the company's network infrastructure. OnFiber enables the constant flow of uploaded images from the Shutterfly Web site to the photofinishing lab (12/16/03).
- Ninety-four percent of customers surveyed gave OnFiber a satisfacory or above rating in a 2003 customer satisfaction survey (11/24/03).
- After reaching EBITDA positive status in the first quarter of 2003, OnFiber has achieved positive cash flow from operations during the third quarter. The company expects to become profitable and free cash flow positive in the first half of 2004 (11/3/03).

Provide Commerce/ProFlowers
www.proflowers.com

- Provide Commerce announces an initial public offering of 4,334,000 shares of common stock at an initial public offering price of $15.00 per share (12/17/03).
- Provide Commerce launches two new Web sites: Uptown Prime (www.uptownprime.com) and Cherry Moon Farms (www.cherrymoonfarms.com). These two new marketplaces, which offer high-quality products shipped direct from the supplier to the consumer at competitive prices, are the latest perishable product categories from Provide Commerce, which also operates the Proflowers Web site (11/5/03).

Portfolio News

SigmaTel
www.sigmatel.com

- SigmaTel appoints Mike Wodopian as vice president of marketing and business development (12/9/03).
- SigmaTel announces third quarter results for the period ending September 30, 2003. Quarterly revenues were a record $32.7 million, up 66 percent from $19.7 million in the second quarter of 2003, and up 233 percent from $9.8 million for the same period in the fiscal year 2002. Pro forma adjusted net income for the third quarter of 2003 was $7.4 million, representing earnings of $0.24 cents per fully diluted share (10/29/03).

The FeedRoom
www.feedroom.com

- The FeedRoom reports that revenue in 2003 increased by 76 percent over 2002. The company also cut its losses by 50 percent in 2003 versus 2002. The FeedRoom averaged quarterly revenue growth of 9.79 percent through 2003 (12/31/03).
- The Feedroom continues to successfully implement its strategy shift from ad-supported destination (feedroom.com) to technology and business process outsourcing solution for broadband applications. During 2003, the company added several new high profile clients that pay The FeedRoom monthly fees for use of its systems and services: General Motors, AT&T, Bausch & Lomb, Sun Microsystems, Reuters, NBC, Herbalife, Honda, The Knot, and Comcast. In addition, the company advanced strategic relationships with Netscape, Real Networks, and Microsoft (12/31/03).
- Starcom selects The Feedroom's network of media supported sites in the first ever TV style "up front" buy for rich media online advertising (10/31/03).

Executive Recruiting

Highlighting key job opportunities at our portfolio companies

LogLogic
(Sunnyvale, CA)
www.loglogic.com

- CEO
- Vice President, Marketing
- Vice President, Sales

Matrix Semiconductor
(Santa Clara, CA)
www.matrixsemi.com

- CFO

Xambala (San Jose, CA)
www.xambala.com

- Vice President, Sales

Conference Calendar

OFC 2004
February 24–26
Los Angeles, CA
Participating: Lynx Photonic Networks, NP Photonics

BIOMEDICAL OPTICS
February 24–26
San Jose, CA
Participating: NP Photonics

NEMAT CONFERENCE
March 2–4
Grenoble, France
Participating: AmberWave

NETWORK OUTLOOK
March 9–10
Redwood City, CA
Participating: Ikanos

FAST NET FUTURES
March 28–April 1
Santa Clara, CA
Participating: Ikanos

ELECTRONICAUSA (ESC)
March 30–April 1
San Francisco, CA
Participating: Jungo

STORAGE NETWORKING WORLD
April 5
Phoenix, AZ
Participating: CreekPath

NGN POLICY
April 19–21
Washington, DC
Participating: Ikanos

STORAGE DECISIONS
April 26
New York, NY
Participating: CreekPath

IDC
May 20
London, England
Participating: CreekPath

IEEE INTERNATIONAL MICROWAVE SYMPOSIUM (MTT)
June 6–11
Fort Worth, TX
Participating: Xpedion

41ST DESIGN AUTOMATION CONFERENCE (DAC)
June 7–11
San Diego, CA
Participating: Xpedion

GARTNER PLANET STORAGE
June 9
Las Vegas, NV
Participating: CreekPath

SUPERCOMM
June 20–24
Chicago, IL
Participating: Ikanos

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